What is claimed is:

1. An orthogonal frequency division multiplexing receiver comprising:

a converter configured to generate a transform signal by Fourier transform of a received signal;

a first interpolator configured to detect a pilot signal from the transform signal, and to provide time interpolation to the pilot signal;

an interference detector configured to provide arithmetic processing to the time interpolated pilot signal, and to detect interference by comparing a result of the arithmetic processing with a threshold;

a second interpolator configured to provide frequency interference interpolation with respect to the interference detected pilot signal, and to provide frequency interpolation to the pilot signal after the interference interpolation; and

a demodulator configured to perform demodulation based on the transform signal and the frequency interpolated pilot signal.

2. The orthogonal frequency division multiplexing receiver of claim 1, wherein the converter comprises:

a quadrature detector configured to generate a baseband signal from the received signal; and

a fast Fourier transform circuit configured to generate the transform signal from the baseband signal.

3. The orthogonal frequency division multiplexing receiver of claim 1, wherein the first interpolator comprises:

a pilot signal detector configured to detect the pilot signal contained in the transform signal; and

a time interpolator configured to interpolate the pilot signal in time direction.

4. The orthogonal frequency division multiplexing receiver of claim 1, wherein the second interpolator comprises:

an interference interpolator configured to subject the time interpolated pilot signal to the interference interpolation in the frequency direction; and

a frequency interpolator configured to provide the frequency interpolation to the pilot signal after the interference interpolation.

5. The orthogonal frequency division multiplexing receiver of claim 1, wherein the interference detector comprises:

a difference operator configured to calculate a difference between complex components of adjacent pilot signals in the frequency direction as the arithmetic processing; and

a threshold comparator configured to compare the difference with the threshold.

6. The orthogonal frequency division multiplexing receiver of claim 5, further comprising a mean value calculator configured to control the threshold in accordance with the difference.

7. The orthogonal frequency division multiplexing receiver of claim 6, wherein the mean value calculator comprises:

a sum-square calculator configured to calculate an amplitude of the pilot signal by providing a sum-of-squares operation to the difference;

an integrator configured to calculate a mean value by integrating the amplitude; and

a correction circuit configured to correct the mean value.

8. The orthogonal frequency division multiplexing receiver of claim 1, wherein the interference detector comprises:

a difference operator configured to calculate a difference between amplitudes of adjacent pilot signals in the frequency direction as the arithmetic processing; and

a threshold comparator configured to compare the difference with the threshold.

9. The orthogonal frequency division multiplexing receiver of claim 1, wherein the interference detector comprises:

a sum-square calculator configured to obtain an amplitude of the pilot signal by executing a sum-of-squares operation as the arithmetic processing; and

a threshold comparator configured to compare the amplitude with the threshold.

10. The orthogonal frequency division multiplexing receiver of claim 9, wherein the threshold comparator determines the interference when the amplitude is greater than an upper limit of the threshold or when the amplitude is smaller than a lower limit of the threshold.

11. The orthogonal frequency division multiplexing receiver of claim 1, further comprising an interference counter configured to count the interference detected pilot signal and to stop the interference interpolation in accordance with the count.

12. The orthogonal frequency division multiplexing receiver of claim 11, wherein the interference detector comprises:

a difference operator configured to calculate a difference between complex

components of adjacent pilot signals in the frequency direction as the arithmetic processing; and

a threshold comparator configured to compare the difference with the threshold.

13. The orthogonal frequency division multiplexing receiver of claim 11, wherein the interference detector comprises:

a difference operator configured to calculate a difference between amplitudes of adjacent pilot signals in the frequency direction as the arithmetic processing; and

a threshold comparator configured to compare the difference with the threshold.

14. The orthogonal frequency division multiplexing receiver of claim 11, wherein the interference detector comprises:

a sum-square calculator configured to obtain an amplitude of the pilot signal by executing a sum-of-squares operation as the arithmetic processing; and

a threshold comparator configured to compare the amplitude with the threshold.

15. The orthogonal frequency division multiplexing receiver of claim 1, further comprising an interference counter configured to count the interference detected pilot signal and to modify the threshold in accordance with the count.

16. The orthogonal frequency division multiplexing receiver of claim 15, wherein the interference detector comprises:

a difference operator configured to calculate a difference between complex components of adjacent pilot signals in the frequency direction as the arithmetic processing; and

a threshold comparator configured to compare the difference with the threshold.

17. The orthogonal frequency division multiplexing receiver of claim 15, wherein the interference detector comprises:

a difference operator configured to calculate a difference between amplitudes of adjacent pilot signals in the frequency direction as the arithmetic processing; and

a threshold comparator configured to compare the difference with the threshold.

18. The orthogonal frequency division multiplexing receiver of claim 15, wherein the interference detector comprises:

a sum-square calculator configured to obtain an amplitude of the pilot signal by executing a sum-of-squares operation as the arithmetic processing; and

a threshold comparator configured to compare the amplitude with the threshold.

19. A semiconductor integrated circuit comprising:

a converter integrated on a semiconductor chip and configured to generate a transform signal by Fourier transform of a received signal;

a first interpolator integrated on the semiconductor chip and configured to detect a pilot signal from the transform signal, and to provide time interpolation to the pilot signal;

an interference detector integrated on the semiconductor chip and configured to provide arithmetic processing to the time interpolated pilot signal, and to detect interference by comparing a result of the arithmetic processing with a threshold;

a second interpolator integrated on the semiconductor chip and configured to provide frequency interference interpolation with respect to the interference detected pilot signal, and to provide frequency interpolation to the pilot signal after the interference interpolation; and

a demodulator integrated on the semiconductor chip and configured to perform demodulation based on the transform signal and the frequency interpolated pilot signal.

20. An orthogonal frequency division multiplexing method for receiving a signal comprising:

generating a transform signal by Fourier transform of a received signal;

detecting a pilot signal from the transform signal;

providing time interpolation to the pilot signal;

providing arithmetic processing to the time interpolated pilot signal;

detecting interference by comparing a result of the arithmetic processing with a threshold;

providing frequency interference interpolation with respect to the interference detected pilot signal;

providing frequency interpolation to the pilot signal after the interference interpolation; and

performing demodulation based on the transform signal and the frequency interpolated pilot signal.